PVP 12

Code: EM3T6, EE3T4

II B.Tech - I Semester – Regular Examinations - January 2014

SWITCHING THEORY AND LOGIC DESIGN
(Common for ECM, EEE)

Duration: 3 hours Marks: 5x14=70

Answer any FIVE questions. All questions carry equal marks

1. a) The message below was coded using Hamming code and transmitted through a noisy channel. Decode the message assuming that a single error has occurred in each code word 1001001011100111101100011011. 8 M

   b) Perform the following operations.
   i) 1100.010 – 1000.111
   ii) 87-999 using 2's arithmetic. 6 M

2. a) Reduce the following Boolean expressions to the four literals.
   i) (A′+C)(A′+C′)(A+B+ CD)
   ii) ABCD+ A′ BD+AB C′ D+ A′ D 8 M

   b) Realize an 2 input EX-OR gate using minimum number of 2 input NAND gates. 6 M

3. a) Minimize the given 5 variable function using QM Tabular method

$f = \sum(2, 4, 9, 10, 11, 12, 19, 20, 21, 22, 23, 24, 25, 26, 29, 31)$. 8 M

b) What do you mean by K-Map? What are its advantages and disadvantages? 6 M

4. a) Design a 5 to 32 line decoder using 3 to 8 line decode, active low outputs with 2 active low and one active high enable. 7 M

b) Use a multiplexer having three data select inputs to implement the logic for the function

$F = \sum m(0,1,2,3,4,10,11,14,15)$. 7 M

5. a) Obtain the switching function realized by the given gate method. 7 M

b) Explain the difference between PLA and PAL. 7 M

6. a) Design and implement a BCD counter using JK flip flops. State if it is self starting. 7 M

b) Design a 3 stage shift register which is an universal register. 7 M

7. a) Design a sequence detector with overlapping, the sequence is 10101. Use SR flip flops in the design. 6 M

b) Reduce the number of states in the following state table and tabulate the reduced state table. 8 M

PS	NSIZ	
	x=0	x=1
A	D, 0	H, 1
B	F, 1	C, 1
C	D, 0	F, 1
D	C, 0	E, 1
E	C, 1	D, 1
F	D, 1	D, 1
G	D, 1	C, 1
H	B, 1	A, 1

8. a) Write a brief note on Hazards and races. 7 M

b) Write a brief note on Hazard free realization. 7 M